



*DPW*

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Re application of: Lee et al.  
Application Serial No.: 10/718,191  
Filed: November 20, 2003  
For: Novel Encapsulation Method for SBGA  
Patent No.: Unassigned  
Issue Date: Unassigned

Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

**CERTIFICATE UNDER 37 C.F.R. §3.73(b)  
ESTABLISHING RIGHT OF ASSIGNEE TO TAKE ACTION**

1. The assignee of the entire right, title and interest hereby seeks to take action in the PTO in this matter.

**IDENTIFICATION OF ASSIGNEE**

2. The assignee of this matter is:

**TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY**  
No. 8, Li-Hsin Rd. 6  
Science-Based Industrial Park  
Hsin-Chu, Taiwan, R.O.C., 300-77

**PERSON AUTHORIZED TO SIGN**

3. Daniel R. McClure  
Attorney for Assignee

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4. A chain of title from the inventor(s) to the current assignee is shown below:

- a. From: Hsin-Hui Lee, Pei-Hwa Tsao, Chao-Yuan Su  
To: Taiwan Semiconductor Manufacturing Company  
Recorded in PTO: Reel: 014737 Frame: 0521

**DECLARATIONS**

5. I, the undersigned, have reviewed all the documents in the chain of title of the

☒ application  
☐ patent

matter identified above and, to the best of my knowledge and belief, title is in the assignee identified above.

6. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

7. I, the person signing below, aver that I am empowered to sign this statement on behalf of the assignee.



**Daniel R. McClure, Reg. No. 38,962**

Tel. No. 770-933-9500  
Customer No.: 24504

**THOMAS, KAYDEN, HORSTEMEYER  
& RISLEY, L.L.P.**  
100 Galleria Parkway, Suite 1750  
Atlanta, Georgia 30339-5948

Docket No. 252016-2780

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:

Application No.:

Filed:

Title:



Commissioner for Patents  
Washington, D.C. 20231

**POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST**  
**(REVOCATION OF PRIOR POWERS)**

As assignee of record of each of the patent applications listed in the table of attachment A,

**REVOCATION OF PRIOR POWERS OF ATTORNEY**

all powers of attorney previously given in each of the listed patent applications are hereby revoked, and

**NEW POWER OF ATTORNEY**

the following attorneys/agents are hereby appointed to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number.

000047390

Patent Trademark Office

Please direct all future correspondence and telephone calls to:

**Daniel R. McClure, Reg. No. 38,962**  
**THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.**  
100 Galleria Parkway, Suite 1750  
Atlanta, Georgia 30339  
770-933-9500

**ASSIGNEE OF ENTIRE INTEREST**

**TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.**

8, Li-Hsin Rd. 6


Hsinchu Science Park

Hsinchu, Taiwan 300-77, R.O.C.

**ASSIGNEE CERTIFICATION**

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with Taiwan Semiconductor Manufacturing Company, Ltd., I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date: January 25, 2005

  
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Chien-Wei (Chris) Chou  
Director - Intellectual Property Division


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Attachment A

| No. | Serial No  | TS/ICN       | Application Title   | Filing Date | Assignment (Reel/Frame) |
|-----|------------|--------------|---|-------------|-------------------------|
| 1   | 10/687,178 | TS02-776     | New Method To Reduce CD Non-Uniformity In IC Manufacturing  | 10/16/03    | 014626/0161             |
| 2   | 10/820,320 | TS01-1357B   | Whole Chip ESD Protection   |             | 013155/0802             |
| 3   | 10/736,948 | TS03-222     | Dry Film Remove Pre-Filter System   | 12/16/03    | 014812/0819             |
| 4   | 10/718,191 | TS03-179     | Novel Encapsulation Method For SBGA   | 11/20/03    | 014737/0521             |
| 5   | 10/781,169 | TS03-130/092 | Underfilling Efficiency By Modifying The Substrate Design Of Flip Chips   | 02/18/04    | 015007/0129             |
| 6   | 10/690,995 | TS03-129     | Electrically Programmable Polysilicon Fuse With Multiple Level Resistance And Programming   | 10/22/03    | 014632/0053             |
| 7   | 10/754,835 | TS02-1398    | Method To Reduce A Capacitor Depletion Phenomena  | 01/09/04    | 014897/0115             |
| 8   | 10/822,193 | TS02-1314    | Novel Test Structure For Speeding Stress-Induced Voiding Test And Method Of Using Same  | 04/09/04    | 015207/0683             |
| 9   | 10/798,558 | TS02-1226    | Calibration Standard For Critical Dimension Verification Of Sub-Tenth Micron Integrated Circuit Technology                                    | 03/11/04    | 015086/0116             |
| 10  | 10/696,006 | TS02-1033    | Structure For Reducing Leakage Currents And High Contact Resistance For Embedded Memory And Method For Making Same                            | 10/29/03    | 014660/0568             |
| 11  | 10/762,166 | TS02-716     | Flash Memory Cell With A Unique Split Programming Channel And Reading Channel   | 01/21/04    | 014915/0977             |
| 12  | 10/718,877 | TS02-622     | Endurance Improvement By Sidewall Nitridation Of Poly Floating Gate For Nonvolatile Memory Devices Using Substrate Or Drain-Side Erase Scheme | 11/21/03    | 014737/0550             |
| 13  | 10/758,316 | TS03/492     | Method Of Fabricating A Word-Line Spacer For Wide Over-Etching Window On Outside Diameter (OD) And Strong Fence                               | 01/15/04    | 014907/0961             |
| 14  | 10/793,406 | TS02/1156    | Heuristics For Efficient Supply Chain Planning In a Heterogeneous Production Line   | 03/04/04    | 015053/0921             |
| 15  | 10/719,722 | TS03/373     | Method To Form Flash Memory With Very Narrow Polysilicon Spacing  | 11/21/03    | 014740/0347             |

Date: January 25, 2005

  
Chien-Wei (Chris) Chou  
Director - Intellectual Property Division

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